IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Attorney Docket No. 14328US02)

In the Application of:	**Electronically Filed**
Bhatia	**Dated: September 13, 2007**
Serial No. 10/776,760	
Filed: 2/10/2004	
For: TWO ADDRESS MAP FOR TRANSACTIONS BETWEEN AN X-BIT PROCESSOR AND A Y-BIT WIDE MEMORY	
Examiner: Nguyen	

Group Art Unit: 2187
Confirmation No. 3474

RESPONSE TO OFFICE ACTION OF MAY 15, 2007 AND

REQUEST FOR CONTINUED EXAMINATION

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This correspondence is filed in response to the Office Action of May 15, 2007, with a period of reply through September 15, 2007, pursuant to Assignee's petition for a one month extension. A Request for Continued Examination accompanies this submission. Applicants request entry of the claim amendments and new claim, consideration of the remarks herein, and allowance to the pending claims. This correspondence includes (1) Amendments to the Specification; (2) a Claim Listing; and (3) Remarks.

AMENDMENTS TO THE SPECIFICATION

The heading FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT is deleted.

Paragraph [0002] is deleted.

The heading [MICROFICHE/COPYRIGHT REFERENCE] is deleted.

Paragraph [0003] is deleted.

Paragraph [0023] is amended as follows:

[0023] Referring now to **FIGURE 1**, there is illustrated a block diagram describing an exemplary circuit wherein the present invention can be practiced. The circuit comprises a processor [105Y] 105X, a processor subsystem 105Y, and a bus 110. The processor [105Y] 105X operates on [Y-bit] X-bit data words while the processor subsystem [105X] 105Y operates on [X-bit] Y-bit data words, wherein X>Y, and wherein both X and Y are integer powers of two. For example, in an exemplary case, the processor 105X can operate on 32-bit words, while the processor subsystem 105Y can operate on 16 bit words.